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Serial Concatenation of Binary LDPC Codes with Iterative Decoding

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Abstract

In this paper, a binary serial turbo LDPC code is presented. It represents a serial concatenated LDPC codes separated by interleavers, with iterative decoding. In this work, we aim to investigate the performance evaluation of concatenated code, with reduced complexity and decoding delay, associated with high order constellation using Gray mapping, over Gaussian and Rayleigh channels. Simulation results show that the performance of a serial concatenated LDPC codes is higher than that of single LDPC code with the same code rate and code block length.

Index Terms—*LDPC codes, serial concatenation, iterative decoding, Gray-QAM constellation.*

I. INTRODUCTION

LDPC codes [1, 2], are errors correcting codes, can achieve a high decoding performance close to Shannon limit [3] for a long code. LDPC codes are linear block codes with parity-check matrices *H* that contain only a very small number of non-zero elements. They are decoded iteratively using a graphical representation corresponds to their parity-check matrix [4]. In [5, 2, 6] the first decoding algorithm, called the Sum-Product Algorithm (SPA), is examined.

An interesting fact of LDPC codes approaching the Shannon limits that those high-performance codes are long irregular [7, 8] codes that are coded with non-constant row and column weights. In general, irregular LDPC codes outperform regular LDPC codes.

However, irregular LDPC codes have higher error floor and encoding complexity than regular LDPC codes, and the decoding complexity of binary LDPC codes of dimension *N* is in the order of *O(N)* [9]. Also, certain channels are constrained to use short block codes due to latency or memory constraints, with high performance [24].

One approach to this problem is to reduce the decoding complexity of binary LDPC codes and increase the performance of regular LDPC codes. One possible solution is to use concatenated binary regular LDPC codes. The strategy of concatenated coding is to build powerful error-correcting codes by associating two or more codes with reasonable decoding complexity[11, 12].

Code concatenation of binary irregular LDPC codes is studded before [13, 14, 15]. Original parallel concatenated LDPC codes, called Parallel Concatenated Gallager Codes (PCGCs), was proposed in [16] in which they showed how different component codes with different parameters affect the overall performance in a Gaussian Channel. They restricted their description of PCGC to rate 1/3 codes constructed by combining two rates 1/2 binary irregular LDPC codes without an interleaver.

The authors in [16] showed that the interleaver is not needed for their proposed code. Also, they predicted that the conclusions are easily extended to the case where three or more codes are used, as introduced in [17] in which a serial concatenated irregular LDPC codes, without interleaver, is introduced. In [18] a PCGC was modified to use an interleaver. The interleaver swaps the element positions of the code; i.e.it changes the weight distribution of the code. Thus, it helps increase the minimum distance of the code.

Also, the authors in[19] showed that high performance could be obtained, while fewer requirements of iterations, with a serial concatenated of two binary irregular LDPC codes, with an interleaver. In [20] non-binary LDPC codes were applied in a serial concatenation scheme with an interleaver. The authors in [20] showed that the proposed code scheme outperforms a single non-binary LDPC code. A serial concatenation of non-binary LDPC codes is proposed in [25].

In this paper, we study a serial concatenation of two and three regular binary LDPC codes with different code rates, in which regular LDPC codes interact in a serial concatenation using an interleaver between the component LDPC codes.

This work investigates the performance of the proposed code with a high order constellation such as 16-QAM using Gray mapping, over Gaussian and Rayleigh channels. These systems are used for high-speed data rate that is both limited in power and bandwidth. To satisfy the limitation of the bandwidth, a QAM is used. However, the QAM degrades system performance and requires a high signal-to-noise ratio, and when the power is limited, the use of good error-correcting code is necessary. Therefore, it is interesting to combine a QAM with the proposed code.

The rest of the paper is structured as follows: the binary LDPC encoding is reviewed in Section 2. In section 3, we describe the decoding of LDPC code and the simplified version of SPA, called LLR-SPA, which is used in our simulation. In section 4, the encoding is investigated, and its decoding is studied

in section 5. The performance evaluation of the proposed code and a single LDPC code, with the same code rate and block length, are elaborated in Section 6. Finally, in section 7, we conclude our findings.

II. BINARY LDPC ENCODING

The $(M \times N) - H$ parity-check matrix of a binary LDPC code can be represented graphically by a Tanner graph, which is a bipartite graph with two disjoint nodes: the variable nodes $v_n (n \in \{1, \dots, N\})$ and the check nodes $c_m (m \in \{1, \dots, M\})$. The edges connect these nodes. The connections correspond to the non-zero elements in the parity check matrix. The number of variable nodes M_n and the check nodes N_m corresponds, respectively, to the number of matrix columns N and rows M.

An LDPC code is called regular if w_v, the number of 1's in each column, is constant for every column and $w_c = w_v.(N/M)$, the number of 1's in each row, is also constant for every row. But if the numbers of 1's in each row or column aren't constant, the code is called an irregular LDPC code.

The following matrix is a regular matrix with $w_v = 2$ and $w_c = 4$.

$$H = \begin{pmatrix} 1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 \end{pmatrix}$$

III. BINARY LDPC DECODING

The decoding algorithms use the Tanner graph as support and precede the messages exchanges on the graph edges between the variable nodes and the check nodes. Each node generates and propagates messages to its neighbours based on its current incoming messages except the input message on the edge where the output message sent. Thus, each edge corresponds to a message.

Let $\alpha_{m,n}$ be the soft messages from variable nodes v_n to check nodes c_m and $\beta_{m,n}$ be the soft messages from check nodes c_m to variable nodes v_n. The initial message Λ_n, at the decoder input, sent from variable nodes v_n to check nodes c_m, is a soft output demapping of the received signal $C_n^{'}$.

The initial message can be a priori information: $Pr(v_n = x/C_n^{'}), x \in \{0,1\}$, where $Pr(v_n = x/C_n^{'})$ is the probability that $v_n = x$ given the received signal $C_n^{'}$, or a log-Likelihood Ratio (LLR): $\Lambda_n = log(Pr(v_n = 0/C_n^{'})/Pr(v_n = 1/C_n^{'}))$. For this work, we use an LLR as an initial message because we use LLR-SPA.

❖ *LLR-SUM-PRODUCT ALGORITHM*

The LLRSum-Product Algorithm performs the following operations [22]:

- Initialization

$$\Lambda_n = log(Pr(v_n = 0/C_n^{'})/Pr(v_n = 1/C_n^{'}))$$

Variable node messages

$$\alpha_{m,n} = \Lambda_n$$

- Iterations

- Check node processing

$$\beta_{m,n} = \prod_{n' \in N_m/n} \operatorname{sgn}(\alpha_{m,n'}) 2 \times \tanh^{-1}\left(\prod_{n' \in N_m/n} \tanh \left| \frac{\alpha_{m,n'}}{2} \right| \right)$$

- Variable node processing

$$\alpha_{m,n}^{'} = \Lambda_n + \sum_{m' \in M_n/m} \beta_{m',n}$$

- A posteriori information

$$\tilde{\Lambda} = \Lambda_n + \sum_{m \in M_n} \beta_{m,n}$$

- Decision

$$z_n = \begin{cases} 1, & \tilde{\Lambda}_n < 0 \\ 0, & \tilde{\Lambda}_n \geq 0 \end{cases}$$

Finally, the algorithm stops if $\left(z_{v_j} H^T = 0\right)$ i.e. $z_v = [z_{v_1}, \dots, z_{v_N}]$ is a valid codeword or a maximum number of iterations is reached.

IV. SERIAL TURBO LDPC CODING

The serial turbo LDPC encoder is a serial concatenation of two binary regular LDPC encoders separated by an interleaver noted π. Figure 1 represents the block diagram of a rate R_{sc} serial turbo LDPC encoder [23], where R_{sc} is given by:

$$R_{sc} = R_1 . R_2$$

where R_1 is the code rate of the fist LDPC encoder ENC_1 and R_2 is the code rate of the second LDPC encoder ENC_2.

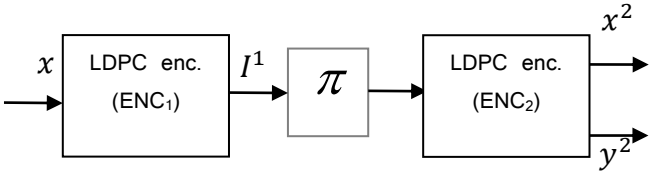

Figure 1. Serial turbo LDPC encoder

The first component encoder ENC_1 encodes the information block d. The second encoder ENC_2 encodes the inerleaved output of the first encoder. Thus, the input of the second encoder is the output of the first encoder.

V. SERIAL TURBO LDPC DECODING

A serial turbo-decoder [23] presented at figure 2, is built of a serial concatenation of two LDPC decoders DEC_1 and DEC_2 associated respectively to the encoders ENC_1 and ENC_2 separated by an interleaver and a deinterleaver noted π^{-1}.

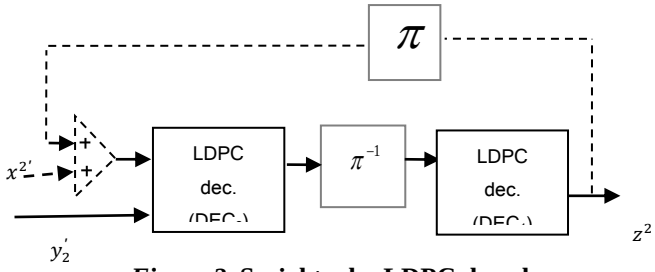

***Figure 2*. Serial turbo LDPC decoder**

Each LDPC decoder is decoded by using a soft-input soft-output decoding algorithm using the "LLRSum-Product Algorithm". The soft outputs from these two component decoders in the decoding process can be again utilized as the soft input to each other's component decoder. Each component decoder communicates its results with the other. Decoding stops at the end of a fixed number of iteration, and the final decision comes from DEC_2. One iteration corresponds to one pass from DEC_1 to DEC_2.

VI. SIMULATION RESULTS

In this section, we discuss the performance of the proposed code using two and three binary LDPC codes; LLR-SPA decodes each one. The proposed code is associated with 16-QAM constellations using Gray mapping over Gaussian and Rayleigh channels.

In figure 3, under Gaussian channel, performance comparison of a single LDPC code, with the parameters $(w_v = 4, M = 1024, N = 1536)$, and a serial concatenation of two LDPC codes: the first encoder is a rate 1/2 LDPC code with the parameters $(w_v = 3, M = 512, N = 1024)$, and the second encoder is a rate 2/3 LDPC code with the parameters $(w_v = 2, M = 512, N = 1536)$ with the same block length 512 bits, the code rate of 1/3 and frame = 50. The maximum number of a single LDPC code is set to 4, and that of the proposed code is set to 2 using one iteration in each component code.

To evaluate the performance of the proposed code in a Rayleigh channel, a performance comparison is conducted on a Rayleigh channel with 16-QAM in figure 4.

The simulation results presented in figures 3 and 4 show that the proposed code outperforms the single LDPC code. As seen in figure 4, the coding gain between a single LDPC code and a serial turbo LDPC code increases in a Rayleigh channel. This means that the interleaver can increase the performance of the proposed code over Rayleigh channel. Also, Turbo LDPC code needs less time delay than a single LDPC code, as shown in table I.

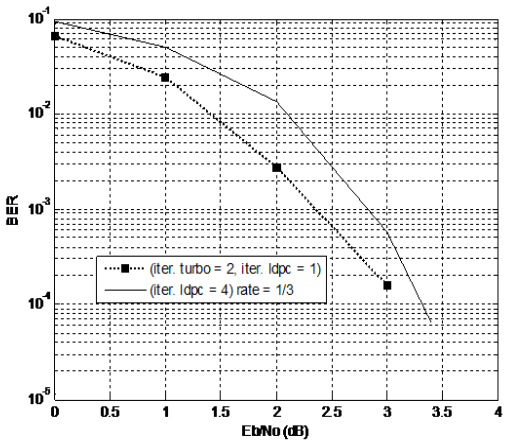

***Figure 3*. Performance comparison of a rate 1/3 serial turbo LDPC code with a rate 1/3 (1024, 1536) LDPC code associated with 16-QAM constellation under Gaussian channel**

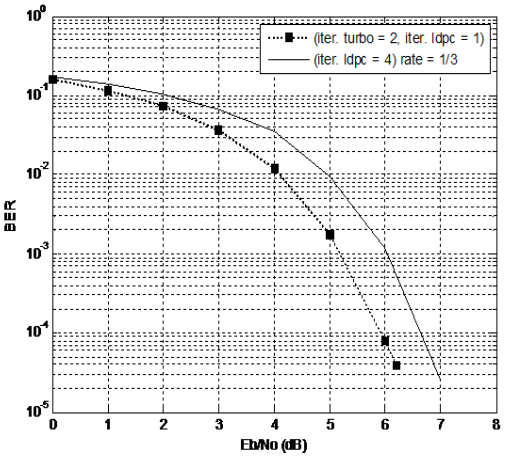

Figure 4. Performance comparison of a rate 1/3 serial turbo LDPC code with a rate 1/3 (1024, 1536) LDPC code associated with 16-QAM constellation under Rayleigh channel

TABLE I. TIME DELAY AND BER COMPARISONS BETWEEN SERIAL TURBO LDPC CODE AND LDPC CODE AT EB/N0 = 3 DB

	LDPC code	*Serial turbo LDPC code*
BER	3.6458e-004	2.3437e-004
Time Delay	16 min, 23.98 s	4 min, 13.93 s

In table I, one can see that the serial concatenation LDPC codes need less time delay than single LDPC code with the same iteration number. It means that the proposed code has not only higher decoding performance, but also it has a lower time delay than a single LDPC code.

In figure 5, under Gaussian channel, with 16-QAM using Gray mapping, a single LDPC code and a serial concatenation of three LDPC codes separated by

interleavers are compared with the same block length 512 bits, the code rate of 1/4 and frame=10.

LDPC code is made by parity check matrix with the parameters $(w_v = 3, M = 1536, N = 2048)$, and serial concatenated LDPC codes are composed of three LDPC codes: the first code is a rate 2/3 LDPC code with the parameters $(w_v = 2, M = 512, N = 1536)$, the second code is a rate 1/2 LDPC code with the parameters $(w_v = 3, M = 512, N = 1024)$ and the third code is a rate 3/4 LDPC code with the parameters $(w_v = 2, M = 512, N = 2048)$. The component LDPC codes and the single LDPC code are decoded by LLR-SPAwith one iteration. The results show that the performance of concatenated LDPC codes is better than that of a single LDPC code.

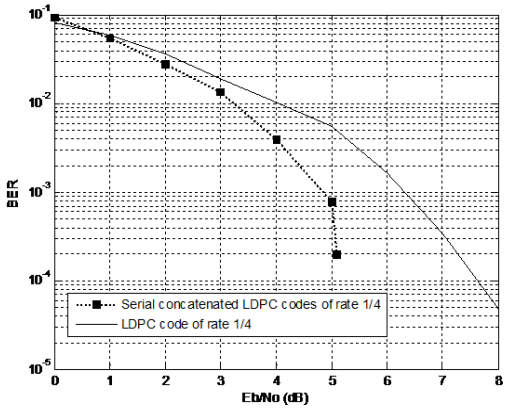

***Figure 5*. Performance comparison of a rate 1/4 serial concatenation of three LDPC codes with a rate 1/4 (512, 2048) LDPC code associated with 16-QAM constellation under Gaussian channel**

VII. CONCLUSION

In this paper, we have proposed a serial concatenation of binary regular LDPC codes separated by interleavers with iterative decoding. This scheme is called binary turbo LDPC codes. The purpose of our work is to avoid the performance weaknesses of LDPC codes, when the block length is small or moderate, or when a high order constellation is used for transmission. Also, we have shown that the proposed code need less time delay than a single LDPC code.

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