

Non-Binary Parallel Turbo LDPC Codes Associated with High Order Constellation

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Abstract

Since the non-binary LDPC (Low-Density Parity-Check) codes offer better performance than binary LDPC codes for a system using high order constellations such as the QAM (Quadrature Amplitude Modulation), one proposes in this paper a high non-binary LDPC code, called a parallel non-binary turbo LDPC code. It is obtained by a parallel concatenation of two identical regular non-binary LDPC codes, separated by an interleaver introducing the diversity through the turbo-code structure proposed by Berrou and others. Regular codes were used to avoid the complexity of irregular codes despite that they have better performance than the regular code. In our simulation, we evaluate over Rayleigh and Gaussian channels, the performance of the proposed code combined with a 16-QAM using Gray mapping. We show that the parallel non-binary turbo LDPC code outperforms a single non-binary LDPC code, with the same code length and code rate. Also, we note that its performance can be improved with the increase of two numbers of iterations: global iterations and iterations of non-binary LDPC codes.

Index Terms—Low-Density Parity-Check codes, turbo-code, parallel concatenation, non-binary, iterative decoding.

I. INTRODUCTION

With the Internet democratization, mobile, user requirements become increasingly large and diverse. So digital communications are an essential solution now. One solution, among others, is to increase the spectral efficiency while guaranteeing an unchanged transmission quality.

Intensive research efforts have been made worldwide to realize the coding solution. The key is to realize a code to get closer to the Shannon limit [1], and also to achieve a good trade-off performance/complexity. Until the 80s, the code that achieves the Shannon limit with reasonable complexity was not yet introduced. Two large error-correcting code families were imposed: the block codes which are subdivided into several types and convolution codes [2].

The performance of a binary code increases with its block length N , while the complexity of decoding a binary code of dimension N is of the order of $O(N)$ [3, 4]. Concatenated codes are introduced to reduce the decoding complexity of a robust error-correcting code.

Concatenated codes are used by Berrou in 1993 [5] to introduce a new code, called turbo-code that can achieve the Shannon limit. Turbo-codes may be block

turbo-codes or convolutional turbo-codes [5, 6] depending on the type of concatenated codes. Thus, depending on the type of concatenation, parallel or serial, we can have parallel or series turbo codes.

After the power of iterative decoding, that was highlighted by the invention of turbo codes. The binary LDPC, which have been neglected because of their complexity, for many years since Gallager introduced them in 1962 [7, 8], have been rediscovered by Mackay [9] in 1995 Spieelman and others [10] in 1996. Luby and others introduced a significant contribution in 1997 [11] which introduced and set the irregular LDPC codes. These later have the main character to perform better than regular code.

In 2002 Davey and Mackey [12] studied the non-binary LDPC codes. These codes are designed in high order Galois Fields $GF(q)$ where q is the cardinality of the Galois field. The non-binary LDPC codes perform better than their binary equivalents when the coded block is low to moderate length, or when the modulation used has high order states. However, the advantages of using non-binary LDPC codes involve a significant increase in decoding complexity. More the high order Galois Fields the complexity becomes essential. For a Galois Field $GF(q)$, the complexity is of order $O(q^2)$. Similarly, the memory required for storing messages is of order $O(q)$.

Also, in [12], the authors proposed the first practical iterative decoding algorithm for non-binary LDPC codes. This algorithm, called the Sum-Product Algorithm (SPA), is optimal iterative decoding with computational complexity. Several algorithms have been proposed to reduce the complexity of the non-binary SPA [13, 14, 15], each one with a particular performance/complexity trade-off, such as FFT-SPA (Fast Fourier Transform), Min-Sum Algorithm, Extended Min-Sum algorithm [16, 17] and the Min-Max Algorithm [41], the Simplified Min-Sum Algorithm [19].

Given the increasing number of applications require high-speed transmission without increasing the bandwidth of the transmission channel, i.e. high spectral efficiency transmissions, while guaranteeing an unchanged transmission quality. This is the reason for the use of a system combining a high-order constellation with high errors correcting code. For this system, the QAM is highly recommended as a high order constellation. So it is interesting to combine a QAM with a non-binary LDPC code.



Although non-binary LDPC codes are valid error-correcting codes for a system using a higher-order constellation, QAM, concatenation of these codes with iterative decoding is still attractive to construct robust errors correcting codes [20, 21, 22] with reasonable complexity.

The original LDPC codes concatenated in parallel PCCGs (Parallel Concatenated Gallager Codes), were introduced in [23] as a class of concatenated codes in which two LDPC codes are irregular binary LDPC codes having different parameters interact in parallel without interleavers. The interleaver runs as a permutation; it changes the weight distribution of the code. It is therefore useful in increasing the minimum distance of the code. In [24, 25], a serial concatenation of binary irregular LDPC codes is also introduced.

The authors in [23] showed how the different components LDPC codes with different parameters affect the overall performance in a Gaussian channel. Although they have limited their description of PCCG to a code rate equals to 1/3 by combining two LDPC codes of code rate equals to 1/2, they predicted that the conclusions are easily extended to the case where three or more codes are used as presented in [24]. Also, in [23] the authors showed that the interleaver is not necessary when the LDPC code is concatenated with another, to study the effect of interleaving between component LDPC codes, has a PCCG been modified to use an interleaver to swap bits of information as in the turbo-code as presented in [26] for irregular codes. However, the irregular LDPC codes have an error floor and a higher coding complexity than regular codes, although they are more efficient than regular code. In [40], the authors introduce the concatenation of binary LDPC codes arranged in parallel through the turbo-code structure proposed by Berrou and others. A serial concatenation of non-binary LDPC codes is proposed in [28].

In this work, we study the concatenation of two identical regular non-binary LDPC codes arranged in parallel through the turbo-code structure proposed by Berrou and others [5], using an interleaver between two LDPC codes that compose it. It is interesting to examine the performance of the proposed code when combined QAM using Gray coding.

The rest of the paper is organized as follows. Section 2 introduces the non-binary LDPC code and the FFT-SPA algorithm used in our simulation. In Section 3 and 4, the parallel turbo LDPC encoding and decoding are investigated, respectively. Finally, the simulation results and concluding remarks are given in Section 5 and 6, respectively.

II. NON-BINARY LDPC CODE

LDPC codes are linear block codes based on low-density parity-check matrices that are to say that the number of non-zero elements of the matrix is much less than the number of 0. The non-zero elements in

the matrix may be binary or non-binary elements. Therefore, we have binary LDPC codes and non-binary LDPC code.

Non-binary LDPC codes are defined by their non-binary parity check matrix H , i.e. the non-zero elements in this matrix are numbers in the Galois field $GF(q)$ ($q > 2$), of size $M \times N$. The entries in the parity-check matrix of a non-binary LDPC code, of size $(N-M)$, belong to $GF(q)$. An encoder output can be expressed as a sequence of symbols in $GF(q)$. Therefore, the code rate is given by $R = (N-M)/N$.

LDPC codes can be regular or irregular according to the regular or irregular distribution of non-zero elements in the matrix. An LDPC code is called regular if the number of non-zeros elements in each columns w_c and/or in each row w_r of the matrix H , is constant. But if the number of non-zeros in each row or column isn't constant, the code is called an irregular LDPC code.

The example of non-binary parity check matrix H of size 4×8 , in the following equation, defined in $GF(4)$, is regular with 2 elements non-zeros per column ($w_c = 2$) and 4 elements non-zeros elements per row ($w_r = 4$).

$$H = \begin{pmatrix} 1 & 0 & 1 & 2 & 0 & 0 & 0 & 4 \\ 2 & 3 & 0 & 1 & 0 & 0 & 2 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 3 & 0 & 0 & 3 & 1 & 1 & 0 \end{pmatrix}$$

Their parity check matrix represents LDPC codes, and by a graphical representation, called the Tanner graph corresponds to the matrix H . The Tanner graph is a bipartite graph composed of two types of nodes: variable nodes representing the symbols of the coded block and the check nodes represent parity check equations. Branches connect these two types of nodes according to the non-zero elements of the matrix H . The number of variables N_m ($m \in \{1, \dots, M\}$) and check nodes M_n ($n \in \{1, \dots, N\}$) corresponds respectively to the number of matrix columns N and rows M .

The Tanner graph is used as a transmission medium by the decoder. At first, all variable nodes are initialized. After, each check node receives messages arriving from the variable nodes that are connected by her branches, then calculates and sends the resulting message that is related to all messages except the input message that the resulting message sent. Then, these same operations are performed by the variable nodes.

Then, a posteriori information associated to each variable node is calculated before taking a decision. Finally, after many iterations or in case the syndrome is zero, the algorithm stops.

Let, for all symbol a , where $a \in GF(q)$, $\alpha_{m,n}$ be the soft messages from variable nodes v_n to check nodes c_m and $\beta_{m,n}$ be the soft messages from check nodes c_m to variable nodes v_n . The initial message γ_n sent from variable nodes v_n to check nodes c_m is a

soft demapping of the received signal γ_n given knowledge of the channel properties.

❖ *FFT-Sum Product Algorithm (FFT-SPA)*

The FFT-SPA can be summarized as follows [29].

- Initialization
 $\gamma_n(a) = Pr(v_n = a/y_n)$
 where $Pr(v_n = a/y_n)$ is the probability that $v_n = a$ given the received signal y_n .
 Variable node messages
 $\alpha_{m,n}(a) = \gamma_n(a)$
 - Iterations

- Check node calculation

$$\beta_{m,n}(h_{ij} \otimes a) = FFT^{-1} \left(\prod_{n \in N_{m/n}} FFT(\alpha_{m,n}(h_{ij} \otimes a)) \right)$$

- Variable node calculation

$$\alpha_{m,n}(a) = \delta_{m,n} \gamma_n(a) \prod_{m' \in M_n/m} \beta_{m',n}(a)$$

$$\text{Where } \delta_{m,n} = \frac{1}{\sum_a \gamma_n(a) \prod_{m' \in M_n/m} \beta_{m',n}(a)}$$

- A posteriori information

$$\tilde{\gamma}_n(a) = \delta_n \gamma_n(a) \prod_{m \in M_n} \beta_{m,n}(a)$$

- Decision

A hard decision is made after each variable node update as:

$$Z_n = \underset{a \in GF(q)}{\operatorname{argmax}}(\tilde{\gamma}_n(a))$$

Finally, after a number of iterations or if

$$Z_{v_j} H^T = 0$$

i.e. $Z_v = [Z_{v_1}, \dots, Z_{v_N}]$ is a valid code word, the algorithm stops.

III. PARALLEL TURBO LDPC CODING

Figure 1 shows the structure of a parallel turbo LDPC code encoder, constructed from two elementary LDPC codes ENC_1 and ENC_2 , separated by an interleaver noted π introducing diversity. This should help increase the free distance of concatenated codes[30].

The code rate of a parallel turbo LDPC code encoder is given by [31]:

$$R_{cp} = \frac{R_1 R_2}{R_1 + R_2 - R_1 R_2}$$

where R_1 is the code rate of the first component encoder ENC_1 and R_2 is the code rate of the second component encoder ENC_2 .

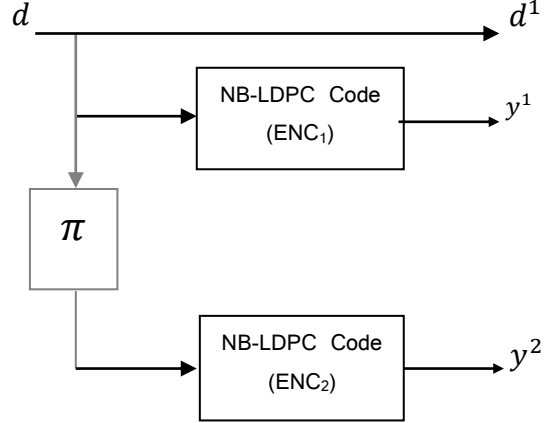


Figure 1. Structure of a rate 1/3 parallel turbo LDPC encoder

The two elementary codes ENC_1 and ENC_2 use the same input blocks, but following different sequences. This is made possible by the presence of the interleaver[32].

Since the two-component encoders are systematic and use the same information block, it does not need to transmit the input of the second encoder C_2 , and this increases the turbo-code efficiency. It is useful only to double the diversity in the presence of fading [33].

Thus, the turbo-encoder rate is 1/3; that is, for every input block, the encoder produces three code blocks. One is the information block itself (we call it the systematic block), and the other two are the parity blocks generated by the two systematic non-binary LDPC encoders[34].

The first elementary code ENC_1 uses the information block of size $N-M$, $d = [d_1 d_2 \dots d_{N-M}]$, with a parity check matrix H of size $M \times N$ and generates the coded information block size N :

$$[y^1 d^1] = [y_1^1 y_2^1 \dots y_M^1 d_1^1 d_2^1 \dots d_{N-M}^1]$$

with d^1 is the systematic block $d^1 = d$, and y^1 is the parity block.

The second elementary encoder ENC_2 uses the interleaved information block $d_{entrelacé}$, and generates the coded block size N :

$$[y^2 d^2] = [y_1^2 y_2^2 \dots y_M^2 d_1^2 d_2^2 \dots d_{N-M}^2]$$

with d^2 is the interleaved information block $d^2 = d_{interleaved}^1 = d_{interleaved}^1$, and y^2 is the parity block.

Therefore, for the information block of a size $N-M$, $d = [d_1 d_2 \dots d_{N-M}]$, the LDPC encoder generates the turbo coded information block of size N :

$$[y^2 y^1 d^1] = [y_1^2 y_2^2 \dots y_M^2 y_1^1 y_2^1 \dots y_M^1 d_1^1 d_2^1 \dots d_{N-M}^1]$$

The parallel concatenation of more than two codes[35] gives turbo codes with low code rates.

IV. PARALLEL TURBO LDPC DECODING

Turbo decoding is done according to the principle of iterative decoding[36] or turbo based on the use of decoders with soft-input and soft-output[37] who exchange reliability information, called extrinsic information, via a cross-reaction, in order to improve the correction over the iterations.

A turbo parallel LDPC decoder shown in figure 2, is constituted by two elementary decoders DEC_1 and DEC_2 respectively associated with ENC_1 and ENC_2 arranged in parallel, two inter leavers and a de-inter leaver noted π^{-1} .

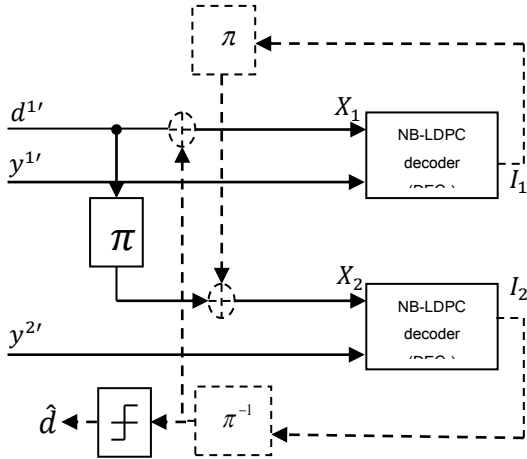


Figure 2. Parallel turbo LDPC decoder

The turbo LDPC decoder contains two LDPC decoders decoded iteratively. Therefore, each iteration $iter_{turbo}$ of the turbo, LDPC code contains multiple iterations $iter_{ldpc}$. The performance of a turbo LDPC code can be improved with the increased number of iterations ($iter_{ldpc}, iter_{turbo}$).

The turbo decoder receives the observations $[y^2, y^1, d^1]$ from the channel and estimates the transmitted message.

Both decoders DEC_1 and DEC_2 work together so that the decoder DEC_1 can benefit from y^2 and the decoder DEC_2 to y^1 . They provide, after a fixed $iter_{ldpc}$, a first estimate I_1 (from DEC_1) and I_2 (from DEC_2), each one communicates its results to the other (I_1 to DEC_2 and I_2 to DEC_1) for a new pass. They then provide a second estimate. After each one communicates its results to the next and so on. Decoding stops after a fixed number of iterations, and the final decision may come from DEC_1 or DEC_2 .

The turbo LDPC decoder receives the soft observations $[y^2, y^1, d^1]$. At each iteration, the two decoders DEC_1 and DEC_2 respectively work together and use the input blocks $[y^1, X_1]$ and $[y^2, X_2]$ with X_1 and X_2 are given by:

$$X_1 = \begin{cases} d^1 \text{ at the first iteration} \\ d^1 + I_2 \text{ deinterleaved at the other iterations} \end{cases}$$

$$X_2 = \begin{cases} d^1 \text{ interleaved at the first iteration} \\ d^1 \text{ interleaved} + I_1 \text{ interleaved at the other iterations} \end{cases}$$

where I_1 and I_2 , the extrinsic information.

The presence of the interleaver π and deinterleaver π^{-1} respectively at the output of the decoder DEC_1 and that of the decoder DEC_2 decorrelate the soft decisions at the output of each decoder [38].

Several methods of interleaving are possible. However, the choice of the structure of an interleaver is a key factor that determines the performance of a turbo LDPC code, in that it changes their free distance property.

So that this turbo LDPC decoder is performed correctly even after several iterations of decoding, interleaving and deinterleaving must be carried out in pseudo-random or random. With these two types of interleaving, turbo LDPC codes appear random. In our work, we use a random interleaver.

In the proposed non-binary turbo LDPC decoder, each non-binary turbo LDPC code contains two non-binary LDPC decoders decoded iteratively. Therefore, each turbo iteration, $iter_{turbo}$ of the non-binary turbo, LDPC code contains multiple LDPC iterations $iter_{ldpc}$. Thus, the total iteration number is:

$$iter_{total} = (iter_{ldpc} \times 2) \times iter_{turbo} \quad [21]$$

V. SIMULATION RESULTS

In this section, we discuss the performance of a rate 1/3 non-binary turbo LDPC code with a parallel concatenation of two identical non-binary LDPC codes constructed on $GF(4)$ of rate 1/2, decoded by FFT-SPA. Note that the simulations here are based on 16-QAM constellations using Gray mapping over Gaussian and Rayleigh channels.

A parity check matrix makes the non-binary LDPC code with the parameters ($w_c = 4, M = 1024, N = 1536$), and the parallel non-binary turbo LDPC code is composed of two identical rates 1/2 non-binary LDPC codes with the parameters ($w_c = 3, M = 512, N = 1024$).

BER performance of a non-binary turbo LDPC code can be improved with the increasing of the iterations number. As mentioned before, the total iteration number is $iter_{total} = (iter_{ldpc} \times 2) \times iter_{turbo}$. Thus, there are many different iteration number settings ($iter_{ldpc}, iter_{turbo}$) can be selected for a fixed $iter_{total}$. We show in figures 3 and 4 the performance improvements of a rate 1/3 (512, 1024)² non-binary turbo LDPC code with several values of iteration.

The results in figure 3 used Gaussian channel show that, with 16-QAM constellation using Gray mapping, the performance comparisons of a rate 1/3 (512, 1024)² non-binary turbo LDPC code with their component code (i.e. a rate 1/2 (512, 1024) non-binary LDPC code and a rate 1/3 (1024, 1536) non-binary LDPC code).

To investigate the performance of a non-binary turbo LDPC code in a Rayleigh fading channel, performance comparisons is conducted on a Rayleigh channel in figure 5.

In figures 3 and 4, we can see that the proposed code outperforms a single non-binary code. We note that, as stated earlier, the performance of a turbo LDPC code can be improved with the increased number of iterations ($iter_{ldpc}, iter_{turbo}$).

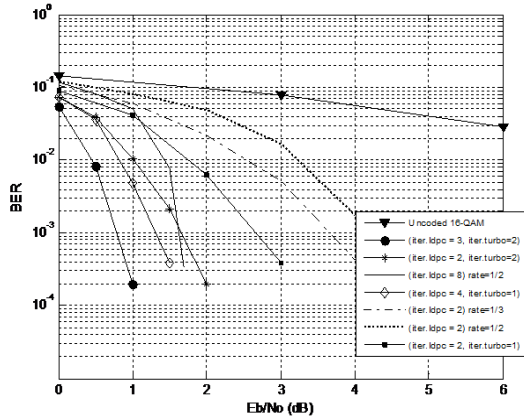


Figure 3. Performance comparisons of a rate 1/3 $(512,1024)^2$ non-binary turbo LDPC code with a rate 1/2 $(512,1024)$ non-binary LDPC code and a rate 1/3 $(1024, 1536)$ non-binary LDPC code, associated with 16-QAM constellation under Gaussian channel.

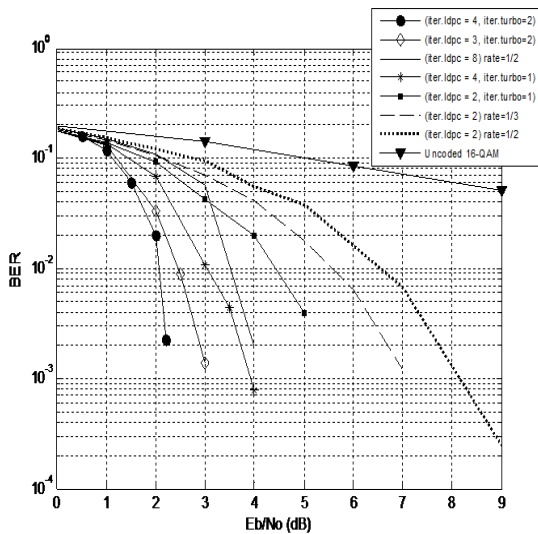


Figure 4. Performance comparisons of a rate 1/3 $(512,1024)^2$ non-binary turbo LDPC code with a rate 1/2 $(512,1024)$ non-binary LDPC code and a rate 1/3 $(1024, 1536)$ non-binary LDPC code, associated with 16-QAM constellation under Rayleigh channel

VI. CONCLUSION

In this work, we propose a non-binary turbo LDPC code. It is an error-correcting code scheme based on the parallel concatenation of non-binary LDPC codes according to the turbo principle proposed by Berrou and other. Simulation results show that the performance of non-binary turbo LDPC code, with [21] Hung, J., Shyu, J. & Chen, S. (2011). "A New High-Performance and Low-complexity Turbo-LDPC Code".

16-QAM constellation using Gray mapping under Gaussian and Rayleigh channels, are higher than their component code and the performance of a rate 1/3 non-binary LDPC code.

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