International Journal of Recent Engineering Science (IJRES),
ISSN: 2349-7157, *volume1 Issue7 July2014*

An Area Efficient Denoising Architecture Using Adaptive Rank Order Filter

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ABSTRACT
Noises are occurs in an images during the process of acquisition and transmission. Image denoising is a process of removing noises from an corrupted images while preserving the details of an image. In existing an decision tree based denoising scheme (DTBDM) and its VLSI architecture is used to remove the impulse noise. The DTBDM consists of two components such as decision-tree-based impulse detector and edge-preserving image filter,these two components are used to detect and remove the noise in an image but this architecture consumes large area.Adaptive rank order filter architecture is proposed to remove the noises and also to reduce area of an architecture.

Index terms*:Adaptive rank order filter, DTBDM, Image denoising, VLSI architecture*

I INTRODUCTION

Image denoising is an important task in image processing and analysis. It can also be applied in Medical imaging and preprocessing for computer vision. In image the noise is present mean, the noise will degrade the performance of an image processing techniques, hence an efficient denoising techniques and its VLSI architecture is used**.** object recognition, object tracking, edge enhancement, edge detection, image segmentation and feature extraction techniques are not perform well in presence of noise in the input image. Image denoising is an important image processing task, both as a process itself, and as a component in other processes. Very many ways to denoise an image or a set of data exists. Depending upon the noisy pixel values present in the image the impulse noise is classified into two types such as fixed valued impulse noise and random-valued impulse noise. The black and white combination of pixel present in an image is fixed valued impulse noise and it otherwise called as salt and pepper noise. There are several denoising scheme is proposed to remove the impulse noise Some of them demage the noisy free pixels and produce very poor results. The median filter[2] removes the impulse noise by changing the luminance values of pixels in image by comparision with median value. This filter produce the poor result if the corrupted pixels in an image is increased. The architecture of this filter is consumes large memory space and area. Usually filter consists of two components such as noise detection and noise filtering.

The image is classified into two types: low complexity image and high complexity image in high complexity the resolution and appearance of image is high,usually the high complexity image used for image processing applications such as medical imaging,printing skills etc.

In existing decision tree based denoising architecture(DTBDM) is used to remove the impulse noise, decision tree is a tree is used to find the status of pixels in an image. The DTBDM architecture consist of two main components such as 1)decision tree based impulse detector**-** It consists of three modules isolation module, fringe module and similarity module.

- Isolation module:It is used to check whether the pixels are in smooth region,if the result is positive means the current pixel is corresponds to noisy pixels otherwise, the pixel is considered as noisy free.
- Fringe module:If the pixel is situated on the edge means the current pixel is corresponds to noisy free pixel,otherwise the pixel is considered as the noisy pixel.
- Similarity module: This module is used to find the similarity between the current pixels and the neighbouring pixel. This module

produce the noisy output when the result is positive.

The another components of an DTBDM architecture is 2) Edge preserving image filter: This filter is used to remove the noisy pixels from an corrupted image and produce the noisy free output.The block diagram of VLSI architecture of decision tree based denoising architecture is shown in Fig1.

II VLSI IMPLEMENTATION OF DTBDM

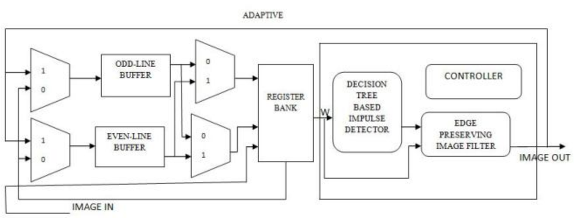

Fig1: Block diagram of VLSI architecture of DTBDM

DTBDM architecture consists of many components such as,

- Line buffer: The line buffer is used to store the pixel values of an input image. The line buffer is further classified into two types 1) Odd line buffer-used to store the odd pixels of an input image 2) Even line buffer-used to store the even pixels of an input image.
- Register bank: The output of the line buffer is get stored on the register bank,it consists of nine register to store the pixel values.
- Decision tree based impulse detector: The architecture of decision tree based impulse detecter consists of three modules to detect the noisy pixels

In VLSI the decision tree based denoising architecture consists of,

Isolation module:

The isolation module architecture consists of CMPL,CMPS comparator units. The CMPL comparatos unit is used to produce the largest value by comparing the two input values whereas,theCMPS produce the smallest value. The comparision output of the first two comparator is applied to the SUB unit, It is used to produce absolute output by making the difference between the two inputs. Finally the GC(greatest comparator) is produce the logic 1 output when the upper input value is greater than the lower one. OR gate is used to generate the binary values of an output.

Fringe module:

The architecture of fringe modules consists FM 1 to FM4 is used to determine its direction,
In implementation of FM_1the E1 is the direction from a to h.Then the SUB units are used to determine the differences between them. Finally the NOR gate is used to produce the result of Fringe module1.

Similarity module:

This module is used to find the similarity between the current pixels and the neighbouring pixels. This module produce the noisy output when the result is positive. In this module we consider two values A,B, if A is greater than B the CO1 is set to 1 otherwise 0.The values from CO1 and CO8 is calculated using the GC units,

This architecture is efficiently removes noise and produce the denoised output, but it also having the drawback that is the consumption of area is large.

III PROPOSED METHOD

In this paper VLSI implementation of Adaptive rank order filter is proposed the proposd scheme overcomes the drawback of the DTBDM.This filter is removes the noise from the highly corrupted image so this filter is an efficient filter when compared to the other filters. The adaptive rank order filter,median filter, order statistics fiter are the type of an non linear filters, the non linear filters are mostly used to remove the noise because the linear filter causes the blur on the image.

The resources required for the implementation of adaptive rank order filter are 1)sliding window module2)Noise detection unit 3)Sorting network4)Median computation unit5) Output selection unit.

The VLSI architecture of an adaptive rank order filter is shown is fig2.

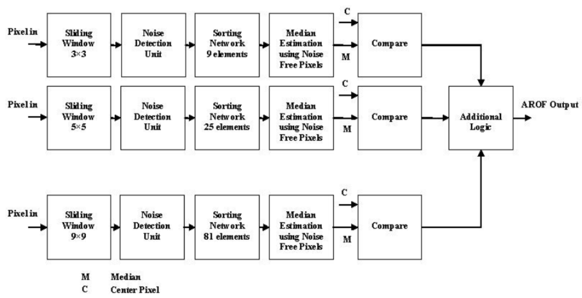

Fig 2:VLSI implementation of AROF

Sliding window module:

The pixels from the input image are loaded serially into the sliding window module. It uses row buffer to read the image pixel and here only one image pixel is read from memory in one clock cycle The pixels are read row by row in a raster scan order.The buffer used here is to reduce the memory access time of pixel per clock cycle.The buffers are choosen depending upon the window size.

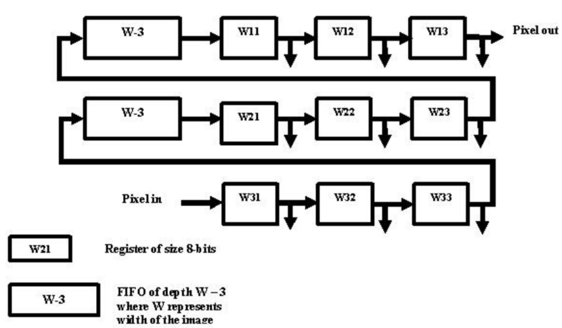

Fig 3:Sliding window module

Noise detection unit:

The pixels from the sliding window module is applied to the noise detection unit.The function of noise detection unit is used to check whether the pixel is corrupted by noise.Finally the output of the noise detection unit is Zero for the noisy input**.**

Sorting network:

The main function of the noise detectionunit is used to sort all the input pixels.This network consists of compare and swap elements, it will depend upon the number of elements to be sorted.

Median computation unit:

This unit is generates the median value for the noise free pixels. The output of the noise detection unit is applied to the input of the median computation unit.

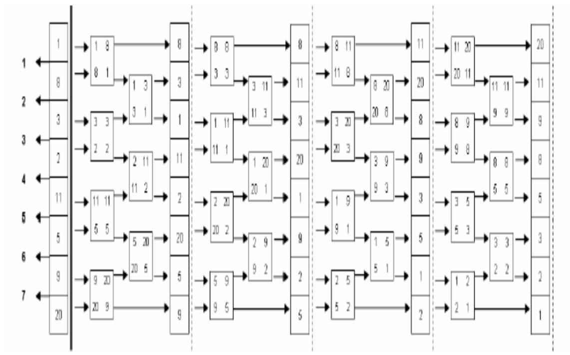

Fig 4: Median Sorter Module

Output selection unit:

This unit is replace the demaged pixels by the median value and the uncorrupted input pixels will be retained.

IV EXPERIMENTAL RESULTS

The architecture of the adaptive rank order filter is implemented in VHDL using the Xilinx ISE simulator version 10.1 tool. The AROF simulation results for 3x3 window is as shown inFig.5

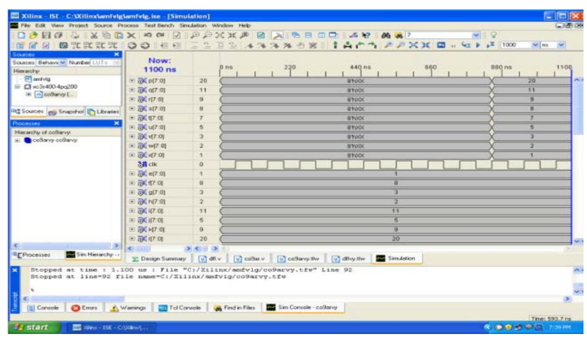

Fig 5: Median Sorter Module for 3x3 window

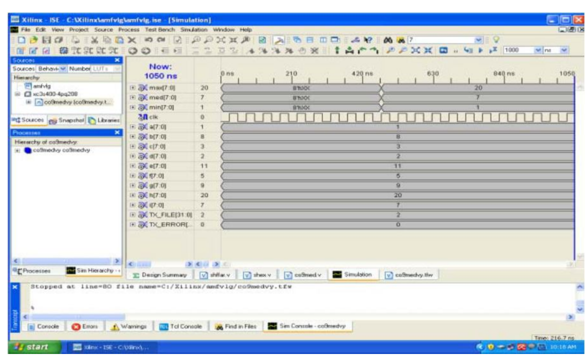

Fig 6:Median Computation for 3x3 window

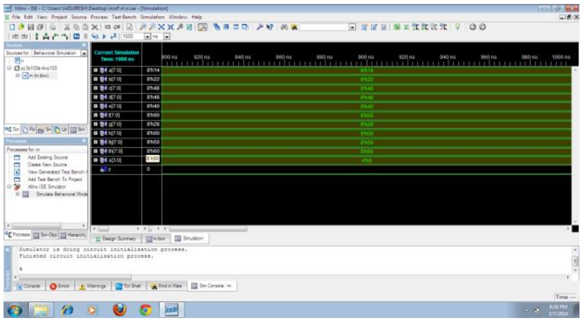

Fig 7: simulation output of AROF architecture

In fig7 shows the simulation output of the adaptive rank order filter. The output o indicates the denoising output.

V CONCLUSION

A low-cost VLSI architecture of the DTBDM architecture is used to remove therandom valued impulse noise.The method uses the decision-tree-based detector to detect the noisy pixel in the image, and employs edge preserving image filter to remove the noisypixels. This architecture consumes large area so an adaptive rank order filter is proposed to remove the impulse noise.AROF is efficiently remove the impulse noise even at the higher noise intensities and this architecture is reduces the area.

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